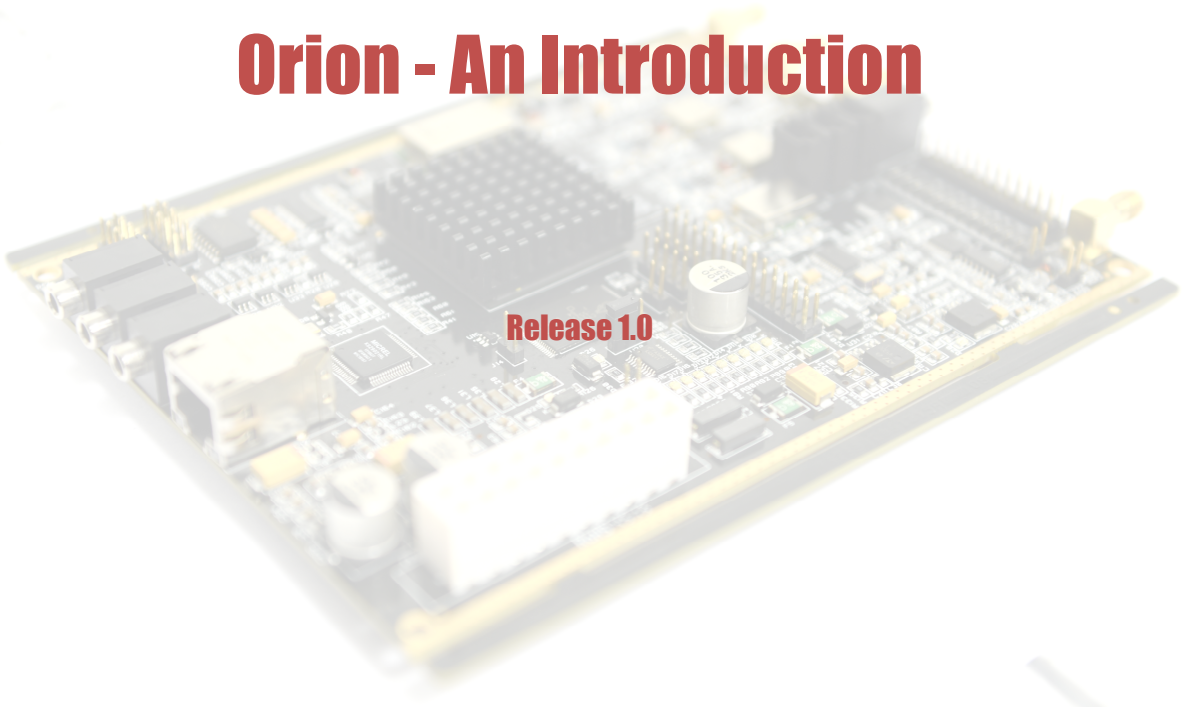
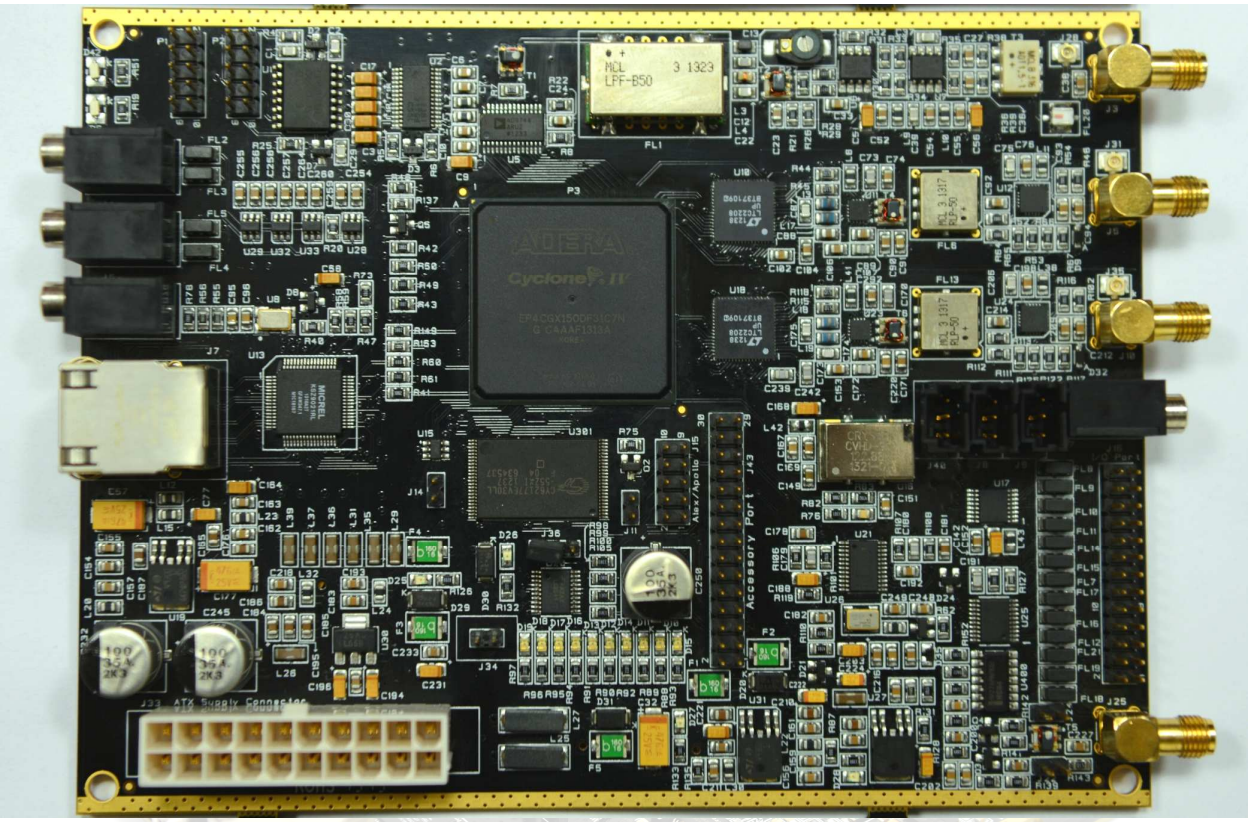
Orion - An Introduction

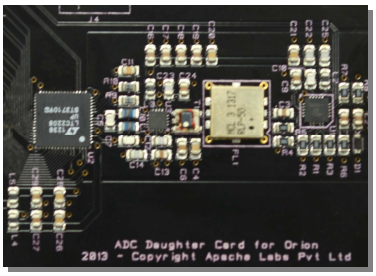


Release 1.0



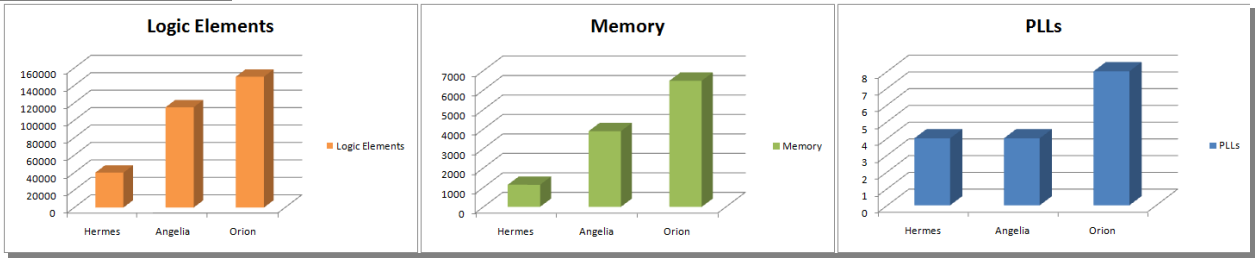
The Orion Software Defined Radio Platform is The most powerful Amateur Radio Transceiver building block available today, it builds on the very successful OpenHPSDR Hermes and the Apache Labs Angelia designs and offers unprecedented performance/functionality not available in any other HF/6M radio transceiver.

There are many firsts that Orion introduces in the HF radio space, this is the first triple phase coherent receive system with an extremely robust and sensitive front end and opens up possibilities of applications such as HFDF, Receiver beam steering to name a few. The third ADC is optional and is implemented via an add on daughter card.



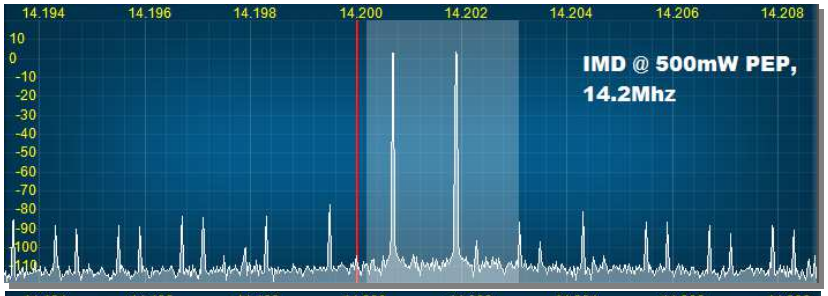
All major controls and settings such as PTT/Mic/Bias/External reference switching is under software control or automated, hence this is an ideal platform for those who would like a consumer plug & play SDR solution.

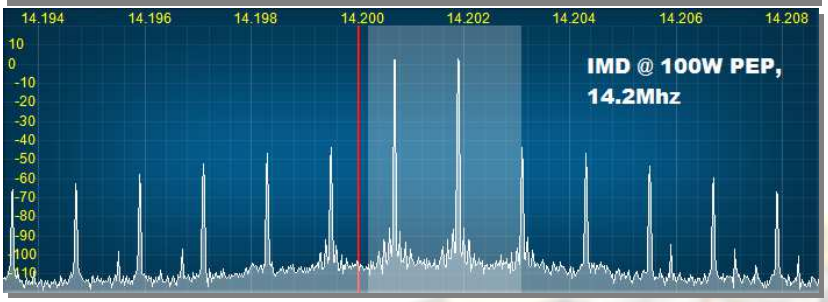
Orion has been designed keeping in mind advanced applications and uses the largest FPGA in any commercially available Amateur Radio SDR, the current implementation uses less than 35% of the resources and has more than adequate headroom for the future applications.



FPGA RESOURCE COMPARISON

The quest for a clean transmitter requires one to either operate in very inefficient Class A mode (at reduced efficiency and power outputs) or invest in a 50v Mosfet design which provides a 10dB improvement in IMD in the best case scenario,





Orion has been designed from the ground up to use modern digital predistortion algorithms to mitigate and reduce the IMD created in the transmitter, 50dB IMD3 has been achieved using Warren's (NR0V) revolutionary new WDSP engine which implements adaptive predistortion,

Implementation of predistortion requires that 40Khz transmit and receive bandwidth be flat within 0.01dB, this amazing feat has been implemented in the FPGA firmware by Phil, VK6PH,

WDSP is currently embedded into PowerSDR(TM), cuSDR and the HPSDR android application,

exceptional transmitter output linearity has been achieved, the results are astounding and far superior to any other Amateur radio transceiver available in the market today, these improvements are also available to the Hermes and Angelia based SDRs.

Like all OpenHPSDR/Apache designs Orion will work on a multitude of software platforms such as :

- The OpenHPSDR flavours of PowerSDR(TM)
- cuSDR
- Kiss Konsole
- John Melton's Android application for OpenHPSDR hardware
- GHPSDR3, GHPSDR3-QT
- GNURADIO- OpenHPSDR

With appropriate software and antennas Orion can be used for :

- HF direction finding
- Rx beam steering using a fixed array of antennas
- 3-antenna interferometry for radio astronomy applications
- Polarization diversity operations (using two of the ADCs) to remove Faraday Rotation effects and to remove polarization misalignment effects during Rx
- Spatial diversity operations to mitigate/reduce signal fading compared with single antenna operations
- Phil Harman, VK6PH's VNA Application
- Alex, VE3NEA's VNA Application

Development Team :

Orion is based on the work of the OpenHPSDR community, the development of this groundbreaking SDR is an example of cross continental teamwork

- Joe Martin, K5SO - Conceptualization of Design, Firmware & beta testing
- Doug Wigley, W5WC - PC software development, integration & beta testing
- Phil Harman, VK6PH - Hardware Design inputs, Orion FPGA Rx/Tx, PHY code based on Phil's work & beta testing
- Abhi Arunoday - Hardware Design, PCB and beta testing
- Warren C Pratt, NR0V - Developer of WDSP, the DSP Processing core used in the Orion SDR

Key Features & Specifications :

- Cyclone IV EP4CGX150 FPGA - 150,000 Logic Elements
- Three Independent phase coherent 16 bit LTC2208 Front Ends (Third via optional daughter card)
- Supports multiple Independent receivers covering 160M through 6M
- 160M - 6M All mode Transmitter (limited only by Software)
- 100W Transceiver based on Orion will be shortly available
- 125dBm Receiver Dynamic Range (All Three Front Ends have identical Dynamic Range)
- Supported sampling rates 48/96/192/384 kHz
- 1.152Mhz of display spectrum with .732 Hz resolution
- Software-selectable 31dB input attenuators in 1dB steps
- Blocking Dynamic Range (ARRL Method) no detectable gain compression below ADC overload
- Transmit and receiver image rejection > 110dB
- Full duplex operation, any split over entire 160m to 6m range
- Extremely Sensitive Receiver, -138dBc MDS @ 14.2MHz, 500Hz bandwidth
- 10MHz 100PPB reference oscillator
- Ultra low phase noise master clock -149dBc @ 10Khz separation
- DUC Transmitter 160M to 6M
- -80dB IMD3 @ 14.2Mhz, 500mW (HF), 250mW (6M) output (with Puresignal enabled)
- -50dB IMD3 @ 14.2Mhz, 100W PEP (with Puresignal enabled) on ANAN-200D
- Automatic 10Mhz internal/external clock switching
- Software controlled Mic, Mic Bias and PTT
- Onboard 128MB Flash
- Onboard 32Mbit Synchronous RAM
- Industry Standard TCP/IP network Ethernet interface supports static, APIPA or DHCP IP address
- FPGA code can be updated via the Industry Standard TCP/IP network Ethernet connection
- Seven user-configurable open-collector outputs, independently selectable per band and Tx/Rx (for relay control, etc - with sequencing via PC code)
- Separate open-collector PTT connection for amplifier control, etc, with sequencer
- Four user-configurable 12 bit analogue inputs (for ALC, SWR etc)
- Three user-configurable digital inputs (for linear amplifier over temperature, etc)
- Low phase noise (-140dBc/Hz @ 1kHz, 14MHz) 122.88MHz master clock, which can be phase-locked to an internal 10MHz 100PPB TCXO or external frequency reference.